

## CLAIMS

What is claimed is:

- 1           1.     A method comprising:  
2     depositing a layer of a metal on a number of conductors disposed on a surface of a wafer;  
3           and  
4     bonding the conductors of the wafer to corresponding conductors on a surface of a second  
5           wafer using the metal layer.
- 1           2.     The method of claim 1, further comprising, prior to depositing the metal  
2     layer on the conductors, removing dielectric material from the surface of the wafer.
- 1           3.     The method of claim 1, further comprising, prior to depositing the metal  
2     layer on the conductors, removing native oxide from the conductors.
- 1           4.     The method of claim 1, wherein the conductors comprise Copper.
- 1           5.     The method of claim 1, wherein the metal comprises one of Silver, Gold,  
2     Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.
- 1           6.     The method of claim 1, wherein the bonding of the conductors of the  
2     wafer to the corresponding conductors of the second wafer is performed at a temperature  
3     between approximately 100 and 300 degrees Celsius.

1           7.     The method of claim 1, wherein depositing the layer of metal on the  
2     conductors comprises:  
3     forming a blanket layer of the metal over the conductors and the surface of the wafer; and  
4     removing the metal from the wafer surfaces.

1           8.     The method of claim 1, wherein depositing the layer of metal on the  
2     conductors comprises selectively depositing the metal on the conductors.

1           9.     The method of claim 8, wherein selectively depositing the metal on the  
2     conductors comprises one of an electroless plating process, an electroplating process, and  
3     a contact displacement plating process.

1           10.    The method of claim 1, wherein the metal layer on each of the conductors  
2     comprises a number of islands.

1           11.    The method of claim 10, wherein the islands are selectively deposited on  
2     the conductors.

1           12.     The method of claim 10, wherein the islands are formed by a process  
2     comprising:  
3     depositing a blanket layer of the metal over the conductors and the surface of the wafer;  
4           and  
5     removing the blanket metal layer from the wafer surface and from portions of each  
6           conductor to form the number of islands on each conductor.

1           13.     A method comprising:  
2     depositing a layer of a first metal on a number of conductors disposed on a first wafer;  
3     depositing a layer of a second metal on a number of conductors disposed on a second  
4           wafer;  
5     aligning the first wafer with the second wafer; and  
6     bonding the metal layer on the conductors of the first wafer with the metal layer on the  
7           conductors of the second wafer.

1           14.     The method of claim 13, further comprising, prior to depositing the metal  
2     layer on the conductors of the first and second wafers, removing dielectric material from  
3     a surface of each of the first and second wafers.

1           15.     The method of claim 13, further comprising, prior to depositing the metal  
2     layer on the conductors of the first and second wafers, removing native oxide from the  
3     conductors of each of the first and second wafers.

1           16.     The method of claim 13, wherein the conductors of each of the first and  
2     second wafers comprise the same metal.

1           17.     The method of claim 16, wherein the conductors of each of the first and  
2     second wafers comprise Copper.

1           18.     The method of claim 13, wherein the first metal and the second metal are  
2     the same.

1           19.     The method of claim 13, wherein the first metal and the second metal are  
2     different.

1           20.     The method of claim 13, wherein each of the first and second metals  
2     comprises one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, and  
3     Platinum.

1           21.     The method of claim 13, wherein the bonding of the conductors of the first  
2     wafer to the corresponding conductors of the second wafer is performed at a temperature  
3     between approximately 100 and 300 degrees Celsius.

1           22.     The method of claim 13, wherein depositing the metal layer on the  
2     conductors of each of the first and second wafers comprises:  
3     forming a blanket metal layer over the conductors and a surface of the wafer; and  
4     removing the blanket metal layer from the wafer surface.

1           23.     The method of claim 13, wherein depositing the metal layer on the  
2     conductors of each of the first and second wafers comprises selectively depositing the  
3     metal layer on the conductors.

1           24.     The method of claim 23, wherein selectively depositing the metal layer on  
2     the conductors comprises one of an electroless plating process, an electroplating process,  
3     and a contact displacement plating process.

1           25.     The method of claim 13, wherein the metal layer on the conductors of at  
2     least one of the first and second wafers comprises a number of islands.

1           26.     The method of claim 25, wherein the islands are selectively deposited on  
2     the conductors.

1           27.     The method of claim 25, wherein the islands are formed by a process  
2     comprising:  
3     depositing a blanket metal layer over each of the conductors and a surface of the wafer;  
4           and  
5     removing the blanket metal layer from the wafer surface and from portions of each  
6     conductor to form the number of islands on each conductor.

1           28.     A wafer stack comprising:  
2     a first wafer including a number of conductors disposed on a surface of the first wafer,  
3           each of the conductors having a layer of metal formed thereon; and  
4     a second wafer including a number of conductors disposed on a surface of the second  
5     wafer, each of the conductors having a layer of metal formed thereon;  
6     wherein the metal layer of each conductor of the first wafer is bonded to the metal layer  
7     on a corresponding conductor of the second wafer.

1           29.     The wafer stack of claim 28, wherein the conductors on each of the first  
2     and second wafers comprise the same metal.

1           30.     The wafer stack of claim 29, wherein the conductors on each of the first  
2     and second wafers comprise Copper.

1           31.     The wafer stack of claim 28, wherein the metal layer on each conductor of  
2     the first wafer and the metal layer on each conductor of the second wafer comprises the  
3     same metal.

1           32.     The wafer stack of claim 28, wherein the metal layer on each conductor of  
2     the first wafer comprises a first metal and the metal layer on each conductor of the second  
3     wafer comprises a second, different metal.

1           33.     The wafer stack of claim 28, wherein the metal layer on each conductor on  
2     each of the first and second wafers comprises one of Silver, Gold, Ruthenium, Osmium,  
3     Iridium, Palladium, Rhodium, and Platinum.

1           34.     The wafer stack of claim 28, wherein the first and second wafers comprise  
2     the same material.

1           35.     The wafer stack of claim 28, wherein the first wafer comprises one  
2     material and the second wafer comprises a different material.

1           36.     The wafer stack of claim 28, wherein the first wafer includes logic  
2     circuitry and the second wafer includes memory circuitry.

1           37.    A wafer stack comprising:  
2    a first wafer, the first wafer having an interconnect including an uppermost dielectric  
3           layer and a number of lower dielectric layers, each lower dielectric layer  
4           including a number of conductors comprised of a first metal and the uppermost  
5           dielectric layer including a number of conductors comprised of a third metal; and  
6    a second wafer, the second wafer having an interconnect including an uppermost  
7           dielectric layer and a number of lower dielectric layers, each lower dielectric layer  
8           including a number of conductors comprised of a second metal and the uppermost  
9           dielectric layer including a number of conductors comprised of a fourth metal;  
10   wherein the conductors comprised of the third metal and the conductors comprised of the  
11           fourth metal are capable of bonding together at a temperature of approximately  
12           300° Celsius or less; and  
13   wherein the conductors of the uppermost dielectric layer of the first wafer are bonded to  
14           the conductors of the uppermost dielectric layer of the second wafer.

1           38.    The wafer stack of claim 37, wherein the first and second metals comprise  
2    the same metal.

1           39.    The wafer stack of claim 38, wherein the first and second metals comprise  
2    Copper.



1           40.    The wafer stack of claim 37, wherein the third and fourth metals comprise  
2 the same metal.

1           41.    The wafer stack of claim 37, wherein each of the third and fourth metals  
2 comprise one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium,  
3 Platinum.

1           42.    The wafer stack of claim 37, wherein the third metal comprises one of  
2 Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, Platinum and the  
3 fourth metal comprises Copper.